

Abstract of the Disclosure

A preferred exemplary embodiment of the current invention concerns a memory testing process, wherein circuitry is provided on a chip to allow on-chip comparison of stored data and expected data. The on-chip comparison allows the tester to transmit in a parallel manner the expected data to a plurality of chips. In a preferred embodiment, at most one address -- and only the column address -- corresponding to a failed memory cell is stored in an on-chip register at one time, with each earlier failed addresses being cleared from the register in favor of a subsequent failed address. Another bit -- the "fail flag" bit -- is stored in the register to indicate that a failure has occurred. If the fail flag is present in a chip, that chip is repaired by electrically associating the column address with redundant memory cells rather than the original memory cells. Subsequently, the chip's register may be cleared and testing may continue. It is preferred that the register and related logic circuitry be configured to avoid storing an address that is already associated with a redundant cell, even though that redundant cell has failed.